John A. Watlington

4 Pinewood Rd
Acton, Massachusetts 01720
wad@alum.mit.edu

Objectives	Architectural design and implementation of media systems

Education

MASSACHUSETTS INSTITUTE OF TECHNOLOGY   *Cambridge, MA*
Candidate for Doctor of Philosophy, ABD.
Thesis title: "MagicEight, An Architecture for Media Processing, and an Implementation"

MASSACHUSETTS INSTITUTE OF TECHNOLOGY   *Cambridge, MA*
Master of Science, September 1989
Thesis title: "Synthetic Movies"

MASSACHUSETTS INSTITUTE OF TECHNOLOGY   *Cambridge, MA*
Bachelor of Science, Electrical Engineering, June 1987
Thesis title: "A Decoder for Vector Coded Color Motion Sequences"

Selected Experience

One Laptop Per Child   *Cambridge, MA*
Vice President of Hardware Engineering   *Feb. 2007—Sept. 2013*
Successfully brought the XO Laptop into production. Responsible for all aspects of laptop production, as well bringing three subsequent generations of laptops into production. Responsibilities included product manager, system architect, lead electrical engineer, and design verification. Also responsible for the initial "school level" software architecture, including centralized school services and software components running on each laptop.
`http://one.laptop.org`

France Telecom Research and Development   *Cambridge, MA*
Principal Research Scientist   *Sept. 2002—Jan. 2007*
Responsible for leading a research team working on creating new applications and services within the networked home, with a goal of analyzing hurdles to deployment, identifying necessary infrastructure, and producing prototypes for early user testing. Other responsibilities included analyzing new technologies and startups in the telecommunications and home networking areas, and working as a liason between MIT and France Telecom. Served as co-chair of a working group within the MIT Communication Futures exploring issues surrounding broadband Internet access.

Ucentric Systems, LLC   *Maynard, MA*
Hardware Guy   *June 2000—August 2002*
Part of small team which defined the second generation product, a residential gateway and home media server system with IP delivery of media content throughout the home. Responsible for the multimedia and hardware portions of the architecture. In 2001 became responsible for managing all hardware development in the company. As lead hardware engineer, planned and oversaw the design and prototype implementation of three system hardware components (the homeserver and clients). As video engineer was responsible for video subsystem design and testing on the first two hardware platforms. Supported business development efforts through quick design/cost estimating of targeted designs for specific customer proposals.

MIT Media Laboratory, Object Based Media Group   *Cambridge, MA*
Research Assistant   *Sept. 1995–May 2000*

Researched object based media, particularly video, exploring both analysis/synthesis techniques and applications, as well as machine architectures for supporting object based media, with a particular interest in reconfigurable processors. Developed a programming model and runtime system (MagicEight) for media processing on heterogeneous parallel processor systems. Based on streams and an extension to hybrid

dataflow, the model is intended to support seamless migration between software and hardware implementations.

MIT Media Laboratory, Television of Tomorrow Group   *Cambridge, MA*
Research Specialist   *Sept. 1989–Aug. 1995*
Participated in research on signal processing and object based video compression. Designed and implemented a multiprocessor motion image processing system (Cheops.) Responsible for initial software simulations, basic architecture specification, and design of the multi-resolution output, memory, and multiprocessor processor modules. In addition to general purpose processors, custom (and reconfigurable) processors specialized for typical media processing tasks were included. Cheops was used as a platform for exploring processing and output intensive tasks such as holographic video and pyramid/wavelet or particle representations of video. Other responsibilities included construction and debugging of the hardware, development of the basic debugging firmware and test software. Supervised procurement, as well as the development of the operating system and runtime resource manager.

                                                                           Cambridge, MA
Consultant   *Nov.–Dec. 1992*
Designed and developed the display system for an interactive art installation, *Genetic Images*, by Karl Sims. The system allowed a single TMC Connection Machine to simultaneously and separately drive sixteen video displays, as well as gathering user feedback.
`http://www.karlsims.com/genetic-images.html`

MIT Media Laboratory, Movies of the Future Group   *Cambridge, MA*
Research Assistant   *June 1987–Aug. 1989*
Worked on digital video subsystems for personal computers. Built a family of full motion video decoders for the IBM PC and Macintosh II (part of Apple's early Quicktime effort) using Vector Quantization. Personally responsible for the hardware design and implementation on both projects, and supervised the software development.

Selected
Publications   John A. Watlington and V. Michael Bove, Jr., *A System for Parallel Media Processing*, Proceedings of the Workshop on Parallel Processing in Multimedia, April 1, 1997.

John A. Watlington and V. Michael Bove, Jr., *Stream-Based Computing and Future Television*, Proceedings of the 137th SMPTE Technical Conference, Sept. 1995.

Edward K. Acosta, V. Michael Bove, Jr., John A. Watlington, and Ross A. Yu, *Reconfigurable processor for a data-flow video processor system*, Proceedings of SPIE #2607 *FPGAs for Fast Board Development and Reconfigurable Computing*, SPIE, Bellingham, WA, Oct. 1995.

V. Michael Bove, Jr., and John A. Watlington, *Cheops: A Reconfigurable Data-Flow System for Video Processing*, IEEE Trans. on Circuits and Systems for Video Technology, Vol. 5, No. 2, April 1995.

John A. Watlington, Mark Lucente, Carlton J. Sparrell, V. Michael Bove, Jr., and Ichiro Tamitani, *A Hardware Architecture for Rapid Generation of Electro-Holographic Fringe Patterns*, Proceedings of SPIE #2406-23 *Practical Holography IX*, SPIE, Bellingham, WA, Feb. 1995.

Background   I am experienced in analog and digital electronics design, manufacturing, and repair, the design of real-time software systems and the software/hardware interface. Other areas of serious study include computer architecture, object-based (and traditional) media formats, image analysis and compression, digital signal processing, printing, and color perception.
`http://watlington.homelinux.org:8000/wad/`